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| **ISCAS High-Level Models**  These pages contain high-level models for all ISCAS-85, several of the smaller ISCAS-89, and several 74X-series circuits. These models may be freely copied and used for research purposes. | http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c499.gif |

http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/cline.gif

**Recent Publication:**

* M. Hansen, H. Yalcin, and J. P. Hayes, "Unveiling the ISCAS-85 Benchmarks: A Case Study in Reverse Engineering," IEEE Design and Test, vol. 16, no. 3, pp. 72-80, July-Sept. 1999.

Abstract: Digital designers normally proceed from behavioral specification to logic circuit; rarely do they need to go in the reverse direction. One such situation is examined here: recovering the high-level specifications of a popular set of benchmark logic circuits. The authors present their methodology and experience in reverse engineering the ISCAS-85 circuits. They also discuss a few of the practical uses of the resulting high-level benchmarks, and make them available for other researchers to use.

The high-level ISCAS-85 benchmarks discussed in this paper are available below, and we invite other researchers to use them. The models, of which we have constructed both structural and behavioral versions, partition the original gate-level netlists into standard RTL blocks and identify the functions of these blocks. Together, the gate-level and high-level models form a set of hierarchicical benchmark circuits that have proven to be useful research tools in several areas of digital design, including test generation, timing analysis, and technology mapping. The web documentation for each model consists of annotated circuit schematic diagrams, and executable (simulatable) descriptions written in structural Verilog. The structural models are intended to express the specific high-level structure implicit in the original gate-level designs. In most cases, we also provide behavioral Verilog models, which define high-level blocks in the form of logical equations that can readily be synthesized into gates.

http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/cline.gif

**ISCAS-85 Circuits:**

* + [c432](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c432.html) : 27-channel interrupt controller
  + [c499/c1355](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c499.html) : 32-bit SEC circuit
  + [c880](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c880.html) : 8-bit ALU
  + [c1908](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c1908/c1908.html) : 16-bit SEC/DED circuit
  + [c2670](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c2670/c2670.html) : 12-bit ALU and controller
  + [c3540](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c3540/c3540.html) : 8-bit ALU
  + [c5315](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c5315/c5315.html) : 9-bit ALU
  + [c6288](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c6288.html) : 16x16 multiplier
  + [c7552](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c7552/c7552.html) : 32-bit adder/comparator

**ISCAS-89 Circuits:**

* + [s208.1](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s208_1.html) : fractional multiplier
  + [s298](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s298.html) : traffic light controller
  + [s344/s349](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s344.html) : 4x4 add-shift multiplier

**74X-Series Circuits:**

* + [74182](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74182.html) : 4-bit carry-lookahead generator
  + [74283](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74283.html) : 4-bit adder
  + [74181](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74181.html) : 4-bit ALU
  + [74L85](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74L85.html) : 4-bit magnitude comparator

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